WHITE PAPER

Technologies for responding to rapid developments in cognitive RF and EW

abaco SYSTEMS

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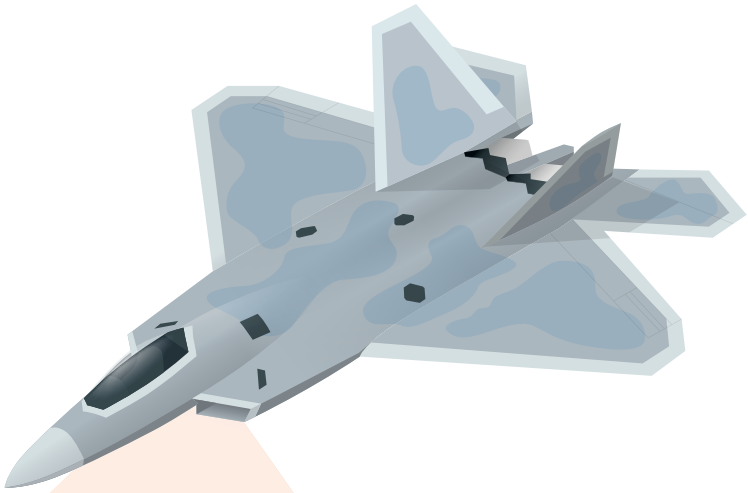

Introduction

Whether it's something as trivial as a business traveler trying to find Wi-Fi at an airport without falling victim to a spoof network, or something as important as a warfighter trying to send positional data in a jammed environment, taking or retaining control of the electromagnetic spectrum in hostile terrain is becoming increasingly important.

For many business travelers, their phone includes a number of techniques to improve signal quality based on the spectrum available - but they also develop their own set of heuristics based on previous experience. Some of these are environmental (there's a café; there will probably be good Wi-Fi signal there); some are based on experience (don't connect to a hotspot called "Jim's big phone"); and some need to be developed on the fly (this looks like a hotel hotspot but the login page seems odd, I'm not going to use it just in case).

What these travelers are essentially doing is a process of sense, learn, and adapt – something that's at the heart of current research into cognitive RF and cognitive EW.

The need for speed

The increased movement in radar and EW systems away from fixed analog systems towards fully digitally programmable systems has allowed both to increase their operational frequency ranges, using frequency agility or advanced modulation techniques. For radar systems, these techniques mean that they are harder to detect but also harder to jam or spoof.

These new methodologies, often described as cognitive RF and cognitive EW, rely on reconfigurable hardware and software that can detect, learn about, and adapt to new threats in the field during a mission.

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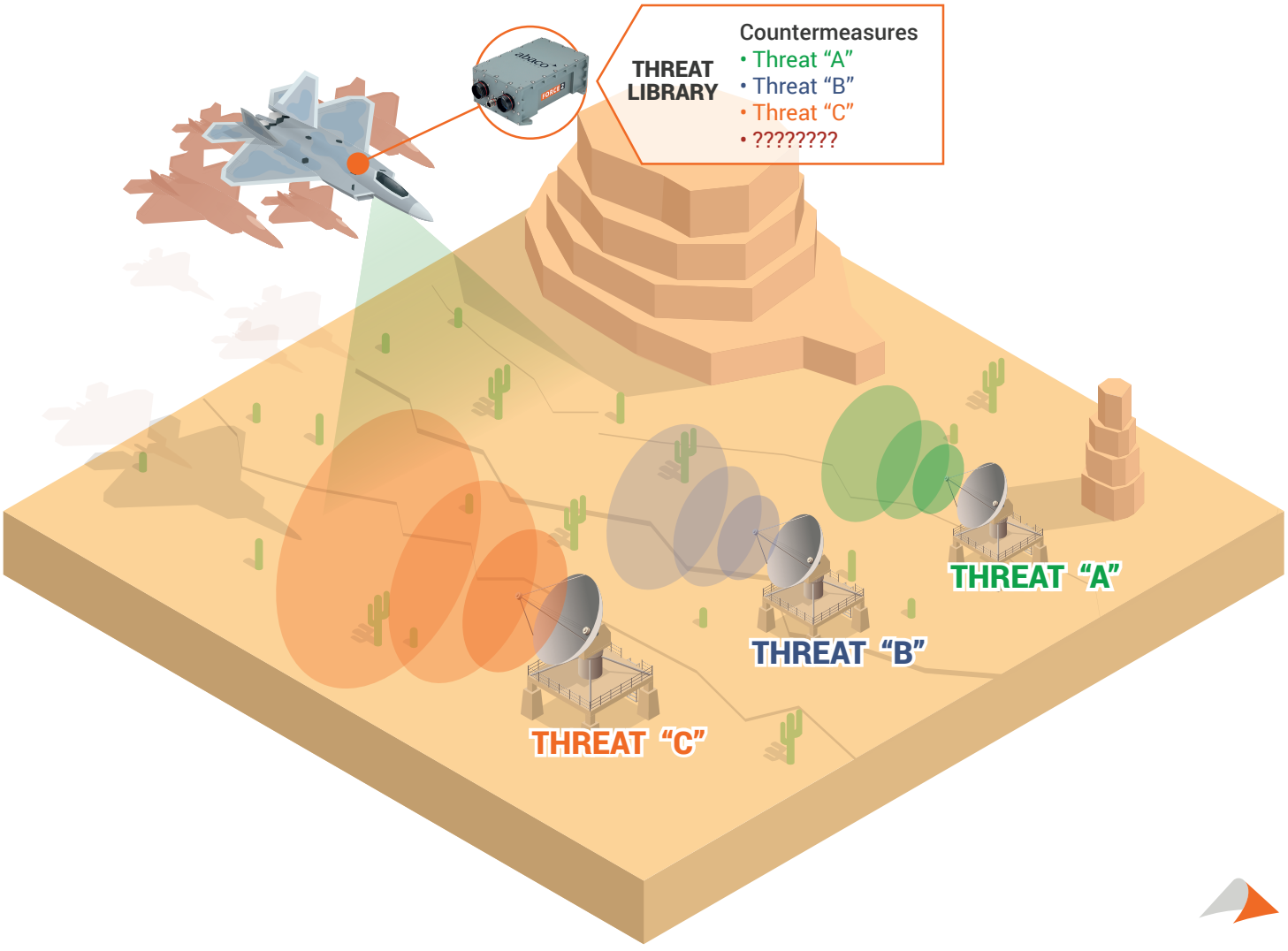
As radars leverage wider bandwidths, jamming and interference technologies also need to increase their operational frequency ranges. The net result is a processing power and bandwidth escalation race, one that is becoming increasingly fast paced.

Traditionally, radar and EW systems have used countermeasures based on a static threat library. There were a number of known threats that the system had been thoroughly tested against - and a proper set of procedures and methods for getting around them.

If an unknown threat was detected, some generic countermeasures could be employed – but, in general, information was gathered on the new threat for post-mission analysis. Further analysis was then conducted over time until an update to the static threat library could be performed and tested. The process could take months, or even years. This methodology was fine when the upgrade process for the threats followed a similar timetable. However, modern digital technology allows threats to quickly employ new techniques. This requires countermeasures to do the same.

These new methodologies, often described as cognitive RF and cognitive EW, rely on reconfigurable hardware and software that can detect, learn about, and adapt to new threats in the field during a mission. To enable this, the learn and adapt process for the threat library becomes a feedback loop, enabling new countermeasures

Static Intelligence Threat Library



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to be developed on the fly. This requires a significant processing performance leap, one that must be accomplished without a significant increase in size, weight, and power.

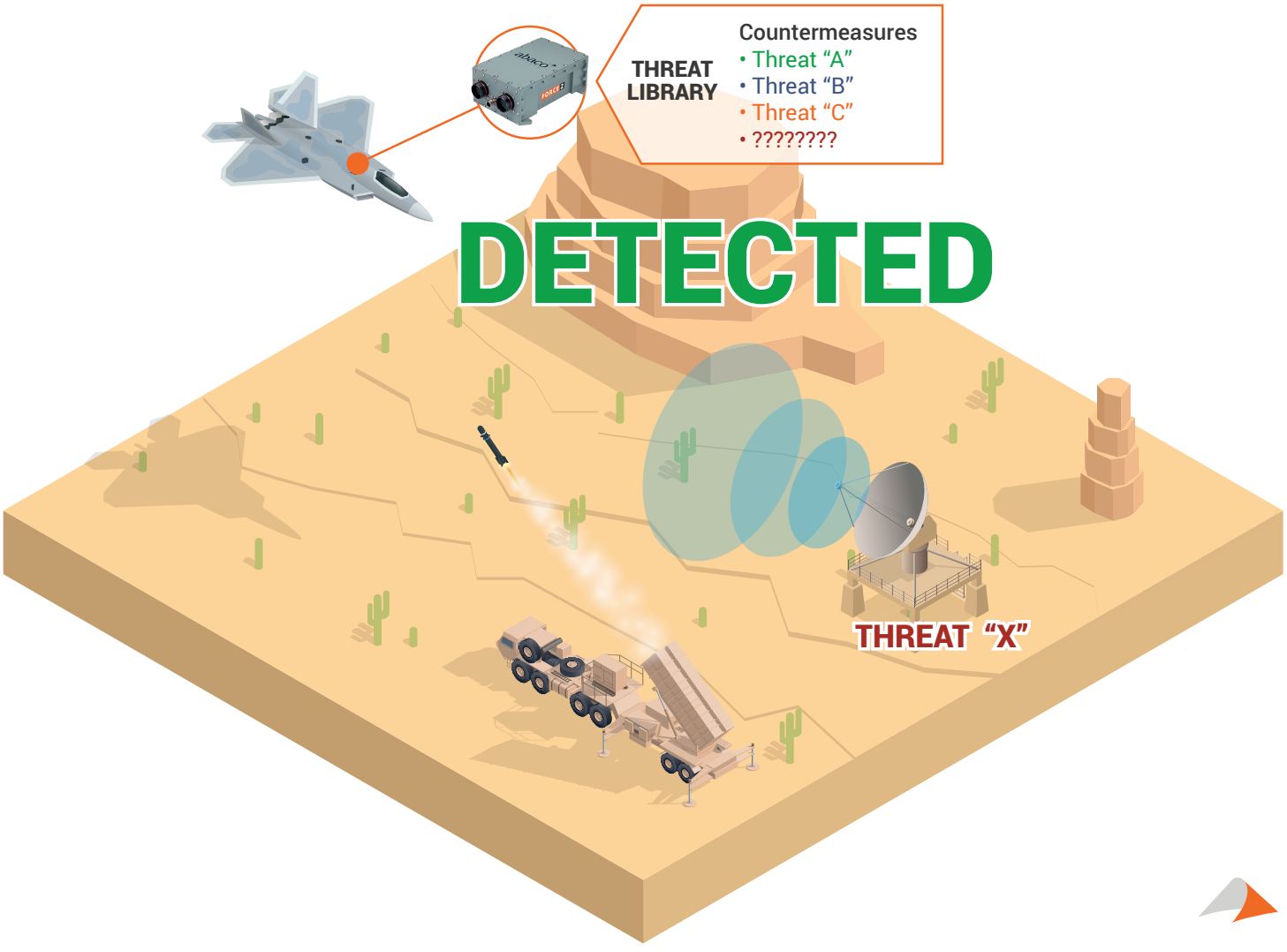
Reconfigurable hardware

A key feature of any prospective cognitive processor is reconfigurability. Algorithms will continue to evolve over time and the best processor architecture for any particular task may change over time. As a result, a multi-processor architecture gives the most flexibility in overcoming evolving threats.

Merely employing a single processor architecture allows some adaptive techniques to be used - but possibly without all. For example, some of the techniques employed may require low latency implementation in field programmable gate array (FPGA) devices while others, such as deep learning based classification, are currently best performed on technologies such as GPUs.

Ideally, the processing unit employs a number of different processing architectures, allowing maximum flexibility for the future. 3U VPX is an ideal platform for this type of work and an example system based on Abaco Systems' boards is shown below. Processor boards based on Intel, NVIDIA GPU, and Xilinx FPGA are readily available and the VPX backplane provides a convenient and rugged mechanism for fast inter-board communication.

Static Intelligence Threat Library



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Optical extensions of the VPX backplane such as VITA 66.4 provide additional protocol-agnostic high speed optical lanes for extra inter-board communication. 3U VPX provides high processing power per Watt, per cubic inch, and per ounce, and solutions can be tailored to every mil/aero environment. In addition, the use of standards based interfaces such as VPX and FMC simplify future hardware upgrades.

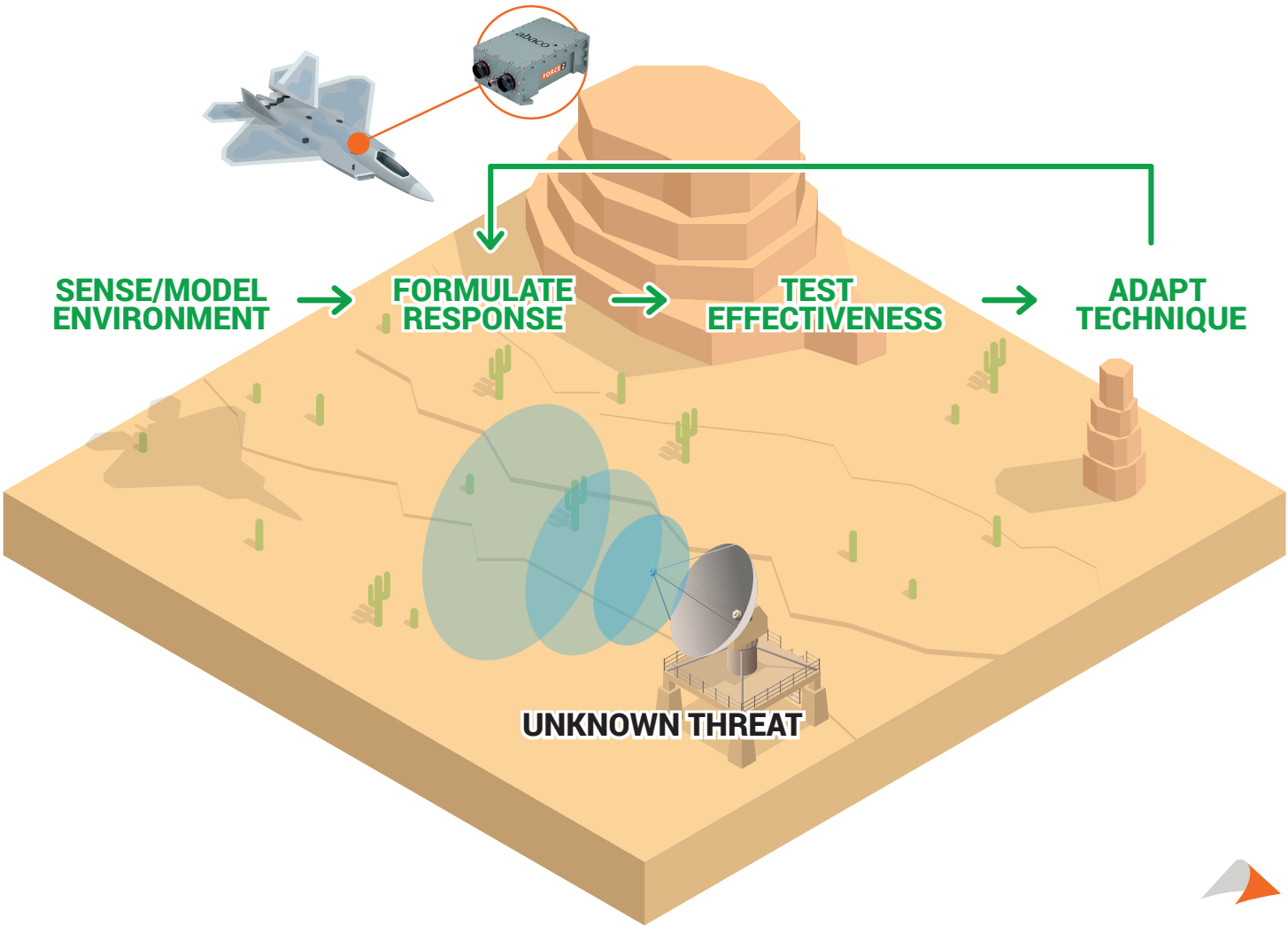
Wanted: low latency processing powerhouse

As we've seen, cognitive systems require multiple channels and wide RF bandwidths – meaning the volume of data that needs to be processed is massive. However, processing architecture is just one of the technology challenges that need to be overcome for modern RF and EW systems. In this section, we consider end-to-end system latency, as data needs to be moved and processed as quickly as possible with minimal buffering or lag between input and output.

The FPGA is a key technology enabler for cognitive systems because of its ability to handle constant streams of high speed data with low latency. As cognitive radar and EW techniques continue to develop, the demand for significant front-end processing resources dramatically increases.

Since cognitive systems often leverage adaptive beamforming and phased arrays, the heavy lifting of signal processing has

Static Intelligence Threat Library



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been moving further and further toward the front-end. Because of its superior ability to undertake stream-based processing using highly-parallel operations, inserting a high-performance FPGA to perform data acquisition and initial signal processing can significantly enhance performance while reducing power consumption and latency. This leaves the less deterministic tasks to either the CPU or GPU on the back end of the system.

Revolutionary technology

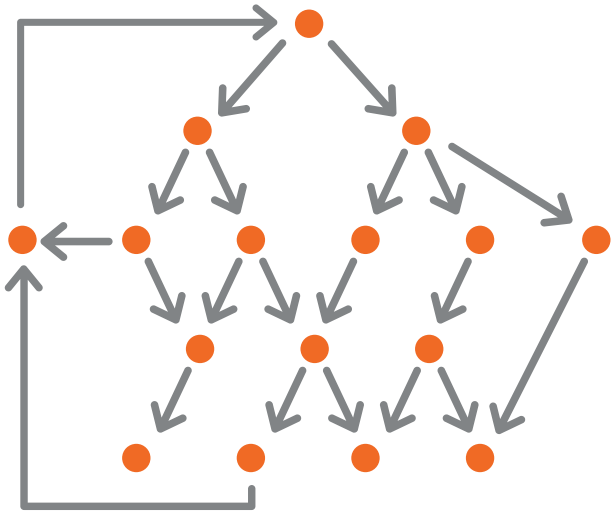
As we established earlier, a bandwidth escalation race is a key component of RF and EW system development, and analog RF performance is key. To overcome this challenge, Abaco's systems take two different approaches to digitizing the necessary data and getting it into the FPGA as quickly as possible. The second of these has only become possible this year.

In many cases, we utilize our industry-leading FMC or FMC+ (VITA 57.1 and VITA 57.4) portfolio of high performance analog-to-digital conversion modules. FMC+ allows the use of modular ADC/DAC boards that employ a low latency interface directly into the high speed transceiver of a modern 3U VPX FPGA carrier such as the VP889, which features a Virtex UltraScale+ FPGA, Zynq Ultrascale+ MPSoC, and an FMC+ site. The use of a mezzanine standard such as FMC+ also enables the ADC card to be easily upgraded so that modern high speed ADC technology from companies like Texas Instruments can allow direct RF sampling.

The second and newer approach is to leverage the revolutionary RFSoC technology from Xilinx, the first FPGA processor to integrate multi giga-sample ADCs and DACs into a SoC architecture. Launched recently, the Zynq Ultrascale+ RFSoC features an integrated ADC, DAC, configurable logic elements, multi-processor embedded ARM Cortex-A53 application processing unit (APU), and an ARM real time processing unit (RPU). This enables input/output channel density to be maximized while reducing the RF signal chain complexity. The benefit is a reduction in system latency and an ideal balance between channel density and signal processing capabilities.

Cognitive EW Computing Requirements

Streaming Computation
Field Programmable Gate Array (FPGA) Polarity



Complex Branching Decision Tree
General Purpose Processor (GPP)
Deep Learning Algorithms
Graphics Processors (GPU)

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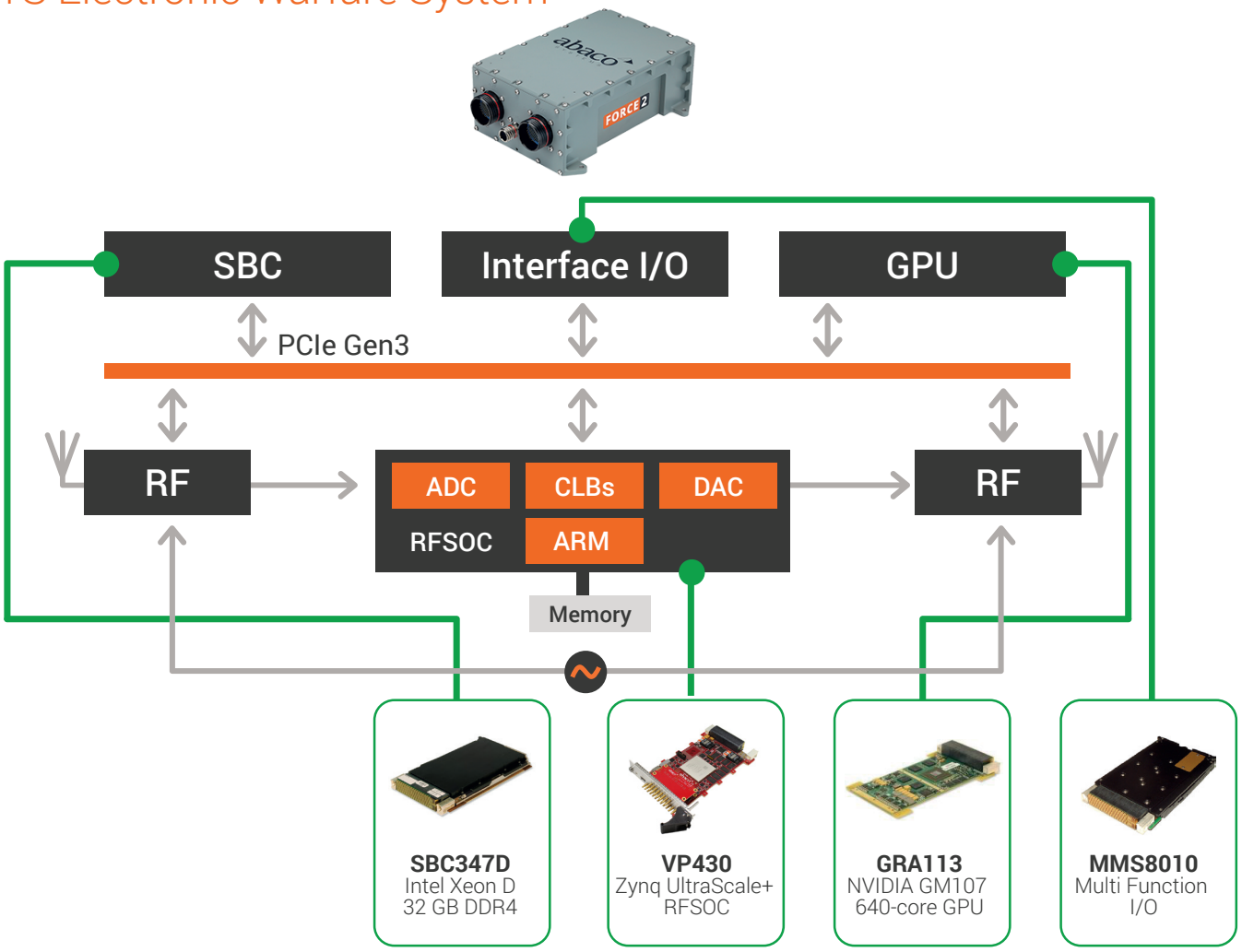
As an example, Abaco's VP430, a 3U VPX RFSoC board, features an integrated 8-channel, 12-bit ADC sampling at 4.0GSPS and 8-channel 14-bit DAC sampling at 6.4GSPS. By reducing the RF signal processing chain, the VP430, with its direct RF sampling 8-channel inputs and 8-channel outputs, minimizes the need for complex up-conversion and down-conversion for many frequency ranges common in radar and electronic warfare. This simplification reduces system latency and enables users to leverage the programmable logic in the FPGA for other tasks that are essential to cognitive countermeasures.

Additionally, the heterogeneous processing capability of the VP430 enables the utilization of the embedded ARM cortex processor for some decision and control processes – optimizing the efficiency of the GPU or CPU, or in some applications, eliminating the need for an additional processor entirely.

When additional processors are still required, there is always the problem of how to handle the extreme volume of data produced when a system includes many channels and extreme sample rates.

COTS Electronic Warfare System



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Many times, a system is limited by the data connection fabric. The VP430 has a traditional VPX data plane interface, allowing a x8 PCIe Gen3 connection to a host computer. With eight ADCs sampling at rates over 6GSPS with two bytes per sample, even the modern PCIe Gen 3 high speed data connection is too slow for a direct transfer.

To overcome this challenge, the VP430 includes – in addition to the PCIe Gen3 data plane - the option to be built with an 8-channel VITA 66.4 fiber optic interface for transfers of greater than 12 GBPS per channel. Previous technologies would have taken four times as many boards to achieve the same level of performance.

Conclusion

Cognitive processing and the constant need for more bandwidth is significantly driving up the performance requirements of radar and EW processing subsystems, while the availability of size, weight, and power is being driven down.

These requirements can be successfully addressed through the use of advanced technologies such as multi-core processors, GPUs, and Xilinx's RFSoC and Zynq MPSoC FPGA, allowing developers to focus on radar prototyping of suitable cognitive and digital processing algorithms. For next generation cognitive radar and EW systems, the VP430 and similar products can provide the necessary edge over adversaries in end-to-end latency and system performance.

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